WHAT IS CLAIMED IS

1. A memory structure comprising:

a source region of a first conductivity type;

a drain region of said first conductivity type;

a first channel region of a second conductivity type opposite said first conductivity type, located adjacent said source region;

a second channel region of said second conductivity type opposite said first conductivity type, located adjacent said drain region;

a transfer channel region of said second conductivity type, located between said first and second channel regions;

a first floating gate located above said first channel region;

a second floating gate located above said second channel region;

a first control gate located above said first floating gate, serving as a steering element associated with said first floating gate;

a second control gate located above said second floating gate, serving as a steering element associated with said second floating gate;

a third control gate located above said transfer channel region, serving as a control gate of an access transistor, said third control gate also overlying at least a portion of said first and second control gates;

a first tunneling zone formed between said first floating gate and said third control gate, and including one or more of edges, side wall, corners of the top edge, portions of the top, and portions of the bottom of said first floating gate; and

a second tunneling zone formed between said second floating gate and said third control gate, and including one or more of

edges, side wall, corners of the top edge, portions of the top, and portions of the bottom of said second floating gate.

2. A memory structure comprising:

a source region of a first conductivity type;

a drain region of said first conductivity type;

a first channel region of a second conductivity type opposite said first conductivity type, located adjacent said source region, a portion of said first channel region adjacent said source region being doped to said second conductivity type to a dopant concentration greater than that of said first channel region;

a second channel region of said second conductivity type opposite said first conductivity type, located adjacent said drain region, a portion of said second channel region adjacent said drain region being doped to said second conductivity type to a dopant concentration greater than that of said second channel region;

a transfer channel region of said second conductivity type, located between said first and second channel regions;

a first floating gate located above said first channel region;

a second floating gate located above said second channel region;

a first control gate located above said first floating gate, serving as a steering element associated with said first floating gate;

a second control gate located above said second floating gate, serving as a steering element associated with said second floating gate;

a third control gate located above said transfer channel region, serving as a control gate of an access transistor;

a first tunneling zone formed between said first floating gate and said third control gate, and including one or more of

edges, side wall, corners of the top edge, portions of the top, and portions of the bottom of said first floating gate; and

a second tunneling zone formed between said second floating gate and said third control gate, and including one or more of edges, side wall, corners of the top edge, portions of the top, and portions of the bottom of said second floating gate.

3. A memory structure comprising:

a source region of a first conductivity type;

a drain region of said first conductivity type;

a first channel region of a second conductivity type opposite said first conductivity type, located adjacent said source region;

a second channel region of said second conductivity type opposite said first conductivity type, located adjacent said drain region;

a transfer channel region of said second conductivity type, located between said first and second channel regions;

a first floating gate located above said first channel region;

a second floating gate located above said second channel region;

a first control gate located above said first floating gate, serving as a steering element associated with said first floating gate;

a second control gate located above said second floating gate, serving as a steering element associated with said second floating gate;

a third control gate located above said transfer channel region, serving as a control gate of an access transistor;

a first tunneling zone formed between said first floating gate and said third control gate, and including one or more of edges, side wall, corners of the top edge, portions of the top, and portions of the bottom of said first floating gate;

a second tunneling zone formed between said second floating gate and said third control gate, and including one or more of edges, side wall, corners of the top edge, portions of the top, and portions of the bottom of said second floating gate;

a first doped region at the interface of said first channel region and said transfer channel region, said first doped region being doped to said second conductivity type and having a greater dopant concentration than that of said first channel region and said transfer channel region; and

a second doped region at the interface of said second channel region and said transfer channel region, said second doped region being doped to said second conductivity type and having a greater dopant concentration than that of said second channel region and said transfer channel region.

4. A memory array having a plurality of memory cells, comprising:

a plurality of diffused lines running in a first direction, serving as source and drain regions of said memory cells, each memory cell having a first channel region located adjacent said source region and a second channel region located adjacent said drain region, and a transfer channel region located between its said first and second channel regions;

a plurality of first floating gates, each located above said first channel region of an associated one of said memory cells;

a plurality of second floating gates, each located above said second channel region of an associated one of said memory cells;

a plurality of first control gate lines, running in said first direction, each located above an associated set of said first floating gates and serving as steering elements associated with each said first floating gate;

a plurality of second control gate lines, running in said first direction, each located above an associated set of said

second floating gates and serving as steering elements associated with each said second floating gate; and

a plurality of row lines, running in a second direction generally perpendicular to said first direction, forming a set of third control gates above said transfer channel regions of each memory cell, overlying at least a portion of associated ones of said first and second control gates and serving as control gates of access transistors of associated memory cells,

wherein each of said memory cells is associated with the intersection of one of said diffused lines and one of said row lines, and

wherein each memory cell includes a first tunnelling zone formed between said first floating gate and said third control gate, and including one or more of edges, side wall, corners of the top edge, portions of the top, and portions of the bottom of said first floating gate, and

wherein each memory cell includes a second tunnelling zone formed between said second floating gate and said third control gate, and including one or more of edges, side wall, corners of the top edge, portions of the top, and portions of the bottom of said second floating gate.

5. A memory array having a plurality of memory cells, comprising:

a plurality of diffused lines running in a first direction, serving as source and drain regions of said memory cells, each memory cell having a first channel region located adjacent said source region, a portion of said first channel region adjacent said source region being doped to said second conductivity type to a dopant concentration greater than that of said first channel region and a second channel region located adjacent said drain region, a portion of said second channel region adjacent said drain region being doped to said second conductivity type to a dopant concentration greater than that of said second channel

region, and a transfer channel region located between its said first and second channel regions;

a plurality of first floating gates, each located above said first channel region of an associated one of said memory cells;

a plurality of second floating gates, each located above said second channel region of an associated one of said memory cells;

a plurality of first control gate lines, running in said first direction, each located above an associated set of said first floating gates and serving as steering elements associated with each said first floating gate;

a plurality of second control gate lines, running in said first direction, each located above an associated set of said second floating gates and serving as steering elements associated with each said second floating gate; and

a plurality of row lines, running in a second direction generally perpendicular to said first direction, forming a set of third control gates above said transfer channel regions of each memory cell, and serving as control gates of access transistors of associated memory cells,

wherein each of said memory cells is associated with the intersection of one of said diffused lines and one of said row lines, and

wherein each memory cell includes a first tunnelling zone formed between said first floating gate and said third control gate, and including one or more of edges, side wall, corners of the top edge, portions of the top, and portions of the bottom of said first floating gate, and

wherein each memory cell includes a second tunnelling zone formed between said second floating gate and said third control gate, and including one or more of edges, side wall, corners of the top edge, portions of the top, and portions of the bottom of said second floating gate.

6. A memory array having a plurality of memory cells, comprising:

a plurality of diffused lines running in a first direction, serving as source and drain regions of said memory cells, each memory cell having a first channel region located adjacent said source region and a second channel region located adjacent said drain region, and a transfer channel region located between its said first and second channel regions;

a first doped region at the interface of each said first channel region and said transfer channel region, said first doped region being doped to said second conductivity type and having a greater dopant concentration than that of said first channel region and said transfer channel region;

a second doped region at the interface of each said second channel region and said transfer channel region, said second doped region being doped to said second conductivity type and having a greater dopant concentration than that of said second channel region and said transfer channel region

a plurality of first floating gates, each located above said first channel region of an associated one of said memory cells;

a plurality of second floating gates, each located above said second channel region of an associated one of said memory cells;

a plurality of first control gate lines, running in said first direction, each located above an associated set of said first floating gates and serving as steering elements associated with each said first floating gate;

a plurality of second control gate lines, running in said first direction, each located above an associated set of said second floating gates and serving as steering elements associated with each said second floating gate; and

a plurality of row lines, running in a second direction generally perpendicular to said first direction, forming a set of third control gates above said transfer channel regions of each

memory cell, and serving as control gates of access transistors of associated memory cells,

wherein each of said memory cells is associated with the intersection of one of said diffused lines and one of said row lines, and

wherein each memory cell includes a first tunnelling zone formed between said first floating gate and said third control gate, and including one or more of edges, side wall, corners of the top edge, portions of the top, and portions of the bottom of said first floating gate, and

wherein each memory cell includes a second tunnelling zone formed between said second floating gate and said third control gate, and including one or more of edges, side wall, corners of the top edge, portions of the top, and portions of the bottom of said second floating gate.

7. A memory structure as in claims 1, 2, 3, 4, 5, or 6 wherein said first conductivity type is N and said second conductivity type is P.

8. A memory structure as in claim 7 wherein said second conductivity type is provided by boron dopants.

9. A memory structure as in claims 1, 2, 3, 4, 5, or 6 wherein said floating gates comprise a first layer of polycrystalline silicon, said first control gates comprise a second layer of polycrystalline silicon, and said third control gate comprises a third layer of polycrystalline silicon.

10. A memory structure as in claims 1, 2, 3, 4, 5, or 6 which is capable of storing two or more logical states.

11. A memory array as in claim 10 wherein said floating gates establish one of a plurality of predetermined charge levels for storing a plurality of two or more logical states.

12. A memory structure as in claims 1, 2, 3, 4, 5, or 6 wherein said source region and said drain region comprise buried diffusions.

13. A memory structure as in claim 12 which further comprises a relatively thick dielectric layer overlying said buried diffusions.

14. A memory structure as in claims 1, 2, 3, 4, 5, or 6 wherein said transfer channel is doped to said second conductivity type to a doped concentration greater than that of first and second channel regions.

15. A memory structure as in claims 1, 2, 3, 4, 5, or 6 wherein said transfer channel is counter doped to said second conductivity type to a net doped concentration less than that of first and second channel regions.

16. A memory array as in claims 4, 5, or 6 organized into a plurality of sectors, each sector comprising one or more rows and organized such that erasure of all cells of a sector is performed simultaneously.

17. A memory array as in claims 4, 5, or 6 organized as a virtual ground array.

18. A memory array as in claims 4, 5, or 6 wherein said one of first or second floating gates in alternate cells in a given row are verified simultaneously.

19. A memory array as in claim 18 wherein an entire row is verified utilizing four verification operations.

20. A memory array as in claims 4, 5, or 6 wherein said one of first or second floating gates of alternate cells in a given row are programmed simultaneously by placing data associated with each memory cell to be programmed on its associated diffused lines.

21. A memory array as in claim 20 wherein an entire row is programmed utilizing four program operations.

22. A method for forming a memory structure comprising the steps of:

forming a source region of a first conductivity type;

forming a drain region of said first conductivity type;

forming a first channel region of a second conductivity type opposite said first conductivity type, adjacent said source region;

forming a second channel region of said second conductivity type, adjacent said drain region;

forming a transfer channel region of said second conductivity type, between said first and second channel regions;

forming a first floating gate above said first channel region;

forming a second floating gate above said second channel region;

forming a first control gate above said first floating gate, serving as a steering element associated with said first floating gate;

forming a second control gate above said second floating gate, serving as a steering element associated with said second floating gate;

forming a third control gate above said transfer channel region, serving as a control gate of an access transistor, said third control gate also overlying at least a portion of said first and second control gates;

forming a first tunneling zone between said first floating gate and said third control gate, and including one or more of edges, side wall, corners of the top edge, portions of the top, and portions of the bottom of said first floating gate; and

forming a second tunneling zone between said second floating gate and said third control gate, and including one or more of edges, side wall, corners of the top edge, portions of the top, and portions of the bottom of said second floating gate.

23. A method for forming a memory structure comprising the steps of:

forming a source region of a first conductivity type;

forming a drain region of said first conductivity type;

forming a first channel region of a second conductivity type opposite said first conductivity type, adjacent said source region, a portion of said first channel region adjacent said source region being doped to said second conductivity type to a dopant concentration greater than that of said first channel region;

forming a second channel region of said second conductivity type, adjacent said drain region, a portion of said second channel region adjacent said drain region being doped to said second conductivity type to a dopant concentration greater than that of said second channel region;

forming a transfer channel region of said second conductivity type, between said first and second channel regions;

forming a first floating gate above said first channel region;

forming a second floating gate above said second channel region;

forming a first control gate above said first floating gate, serving as a steering element associated with said first floating gate;

forming a second control gate above said second floating gate, serving as a steering element associated with said second floating gate;

forming a third control gate above said transfer channel region, serving as a control gate of an access transistor;

forming a first tunneling zone between said first floating gate and said third control gate, and including one or more of edges, side wall, corners of the top edge, portions of the top, and portions of the bottom of said first floating gate; and

forming a second tunneling zone between said second floating gate and said third control gate, and including one or more of edges, side wall, corners of the top edge, portions of the top, and portions of the bottom of said second floating gate.

24. A method for forming a memory structure comprising the steps of:

forming a source region of a first conductivity type;

forming a drain region of said first conductivity type;

forming a first channel region of a second conductivity type opposite said first conductivity type, adjacent said source region;

forming a second channel region of said second conductivity type, adjacent said drain region;

forming a transfer channel region of said second conductivity type, between said first and second channel regions;

forming a first floating gate above said first channel region;

forming a second floating gate above said second channel region;

forming a first control gate above said first floating gate, serving as a steering element associated with said first floating gate;

forming a second control gate above said second floating gate, serving as a steering element associated with said second floating gate;

forming a third control gate above said transfer channel region, serving as a control gate of an access transistor;

forming a first tunneling zone between said first floating gate and said third control gate, and including one or more of edges, side wall, corners of the top edge, portions of the top, and portions of the bottom of said first floating gate;

a second tunneling zone between said second floating gate and said third control gate, and including one or more of edges, side wall, corners of the top edge, portions of the top, and portions of the bottom of said second floating gate;

forming a first doped region at the interface of said first channel region and said transfer channel region, said first doped region being doped to said second conductivity type and having a greater dopant concentration than that of said first channel region and said transfer channel region; and

forming a second doped region at the interface of said second channel region and said transfer channel region, said second doped region being doped to said second conductivity type and having a greater dopant concentration than that of said second channel region and said transfer channel region.

25. A method for forming a memory array having a plurality of memory cells, comprising the steps of:

forming a plurality of diffused lines running in a first direction, serving as source and drain regions of said memory cells, each memory cell having a first channel region located adjacent said source region and a second channel region located

adjacent said drain region, and a transfer channel region located between its said first and second channel regions;

forming a plurality of first floating gates, each located above said first channel region of an associated one of said memory cells;

forming a plurality of second floating gates, each located above said second channel region of an associated one of said memory cells;

forming a plurality of first control gate lines, running in said first direction, each located above an associated set of said first floating gates and serving as steering elements associated with each said first floating gate;

forming a plurality of second control gate lines, running in said first direction, each located above an associated set of said second floating gates and serving as steering elements associated with each said second floating gate; and

forming a plurality of row lines, running in a second direction generally perpendicular to said first direction, forming a set of third control gates above said transfer channel regions of each memory cell, overlying at least a portion of associated ones of said first and second control gates and serving as control gates of access transistors of associated memory cells,

wherein each of said memory cells is associated with the intersection of one of said diffused lines and one of said row lines, and

wherein each memory cell includes a first tunnelling zone formed between said first floating gate and said third control gate, and including one or more of edges, side wall, corners of the top edge, portions of the top, and portions of the bottom of said first floating gate, and

wherein each memory cell includes a second tunnelling zone formed between said second floating gate and said third control gate, and including one or more of edges, side wall, corners of

the top edge, portions of the top, and portions of the bottom of said second floating gate.

26. A method of forming a memory array having a plurality of memory cells, comprising the steps of:

forming a plurality of diffused lines running in a first direction, serving as source and drain regions of said memory cells, each memory cell having a first channel region located adjacent said source region, a portion of said first channel region adjacent said source region being doped to said second conductivity type to a dopant concentration greater than that of said first channel region and a second channel region located adjacent said drain region, a portion of said second channel region adjacent said drain region being doped to said second conductivity type to a dopant concentration greater than that of said second channel region, and a transfer channel region located between its said first and second channel regions;

forming a plurality of first floating gates, each located above said first channel region of an associated one of said memory cells;

forming a plurality of second floating gates, each located above said second channel region of an associated one of said memory cells;

forming a plurality of first control gate lines, running in said first direction, each located above an associated set of said first floating gates and serving as steering elements associated with each said first floating gate;

forming a plurality of second control gate lines, running in said first direction, each located above an associated set of said second floating gates and serving as steering elements associated with each said second floating gate; and

forming a plurality of row lines, running in a second direction generally perpendicular to said first direction, forming a set of third control gates above said transfer channel

regions of each memory cell, and serving as control gates of access transistors of associated memory cells,

wherein each of said memory cells is associated with the intersection of one of said diffused lines and one of said row lines, and

wherein each memory cell includes a first tunnelling zone formed between said first floating gate and said third control gate, and including one or more of edges, side wall, corners of the top edge, portions of the top, and portions of the bottom of said first floating gate, and

wherein each memory cell includes a second tunnelling zone formed between said second floating gate and said third control gate, and including one or more of edges, side wall, corners of the top edge, portions of the top, and portions of the bottom of said second floating gate.

27. A method of forming a memory array having a plurality of memory cells, comprising the steps of:

forming a plurality of diffused lines running in a first direction, serving as source and drain regions of said memory cells, each memory cell having a first channel region located adjacent said source region and a second channel region located adjacent said drain region, and a transfer channel region located between its said first and second channel regions;

forming a first doped region at the interface of each said first channel region and said transfer channel region, said first doped region being doped to said second conductivity type and having a greater dopant concentration than that of said first channel region and said transfer channel region;

forming a second doped region at the interface of each said second channel region and said transfer channel region, said second doped region being doped to said second conductivity type and having a greater dopant concentration than that of said second channel region and said transfer channel region;

forming a plurality of first floating gates, each located above said first channel region of an associated one of said memory cells;

forming a plurality of second floating gates, each located above said second channel region of an associated one of said memory cells;

forming a plurality of first control gate lines, running in said first direction, each located above an associated set of said first floating gates and serving as steering elements associated with each said first floating gate;

forming a plurality of second control gate lines, running in said first direction, each located above an associated set of said second floating gates and serving as steering elements associated with each said second floating gate; and

forming a plurality of row lines, running in a second direction generally perpendicular to said first direction, forming a set of third control gates above said transfer channel regions of each memory cell, and serving as control gates of access transistors of associated memory cells,

wherein each of said memory cells is associated with the intersection of one of said diffused lines and one of said row lines, and

wherein each memory cell includes a first tunnelling zone formed between said first floating gate and said third control gate, and including one or more of edges, side wall, corners of the top edge, portions of the top, and portions of the bottom of said first floating gate, and

wherein each memory cell includes a second tunnelling zone formed between said second floating gate and said third control gate, and including one or more of edges, side wall, corners of the top edge, portions of the top, and portions of the bottom of said second floating gate.

28. A method as in claims 22, 23, 24, 25, 26, or 27 wherein said first conductivity type is N and said second conductivity type is P.

29. A method as in claim 28 wherein said second conductivity type is provided by boron dopants.

30. A method as in claims 22, 23, 24, 25, 26, or 27 wherein said floating gates comprise a first layer of polycrystalline silicon, said first control gates comprise a second layer of polycrystalline silicon, and said third control gate comprises a third layer of polycrystalline silicon.

31. A method as in claims 22, 23, 24, 25, 26, or 27 which is capable of storing two or more logical states.

32. A method as in claim 31 wherein said floating gates establish one of a plurality of predetermined charge levels for storing a plurality of two or more logical states.

33. A method as in claims 22, 23, 24, 25, 26, or 27 wherein said source region and said drain region comprise buried diffusions.

34. A method as in claim 33 which further comprises the step of forming a relatively thick dielectric layer overlying said buried diffusions.

35. A method as in claims 22, 23, 24, 25, 26, or 27 wherein said transfer channel is doped to said second conductivity type to a doped concentration greater than that of first and second channel regions.

36. A method as in claims 22, 23, 24, 25, 26, or 27 wherein said transfer channel is counter doped to said second conductivity type to a net doped concentration less than that of first and second channel regions.

37. A method as in claims 25, 26, or 27 organized into a plurality of sectors, each sector comprising one or more rows and organized such that erasure of all cells of a sector is performed simultaneously.

38. A method as in claims 25, 26, or 27 organized as a virtual ground array.

39. A method as in claims 25, 26, or 27 wherein said one of first or second floating gates in alternate cells in a given row are verified simultaneously.

40. A method as in claim 39 wherein an entire row is verified utilizing four verification operations.

41. A method as in claims 25, 26, or 27 wherein said one of first or second floating gates of alternate cells in a given row are programmed simultaneously by placing data associated with each memory cell to be programmed on its associated diffused line.

42. A method as in claim 20 wherein an entire row is programmed utilizing four program operations.

43. A method as in claims 22, 23 or 24 wherein said steps of forming said first floating gate and said first control gate, and said second floating gate and said second control gate comprising the steps of:

forming a plurality of polycrystalline silicon strips in a first direction above and insulated from said first and second channel regions;

forming a layer of polycrystalline silicon above and insulated from said plurality of polycrystalline silicon strips; and

patterning said plurality of polycrystalline silicon strips and said layer of polycrystalline silicon into strips running in a second direction generally perpendicular to said first direction in order to form said first and second floating gates and said first and second control gates.

44. A method as in claims 25, 26, or 27 wherein said steps of forming said first floating gate and said first control gate, and said second floating gate and said second control gate comprising the steps of:

forming a plurality of polycrystalline silicon strips in said second direction above and insulated from said first and second channel regions;

forming a layer of polycrystalline silicon above and insulated from said plurality of polycrystalline silicon strips; and

patterning said plurality of polycrystalline silicon strips and said layer of polycrystalline silicon into strips running in said first direction in order to form said first and second floating gates and said first and second control gates.

45. A method as in claim 43 wherein said step of patterning said plurality of polycrystalline silicon strips and said layer of polycrystalline silicon is performed using the minimum feature lithographic width available in the fabrication process.

46. A method as in claim 44 wherein said step of patterning said plurality of polycrystalline silicon strips and said layer of polycrystalline silicon is performed using the minimum feature lithographic width available in the fabrication process.

47. A method as in claims 22, 23, 24, 25, 26, or 27 wherein said step of forming said transfer channel region and said source and drain regions comprises the step of delineating said transfer channel region and said source and drain regions simultaneously.

48. A method as in claim 47 wherein said step of simultaneously delineating said transfer channel region and said source and drain regions is performed utilizing the minimum lithographic space between features available in the fabrication process.

49. A method as in claims 22, 23, 24, 25, 26, or 27 which further comprises the step of forming a tunnel oxide on only the edges of said first floating gate and said second floating gate adjacent to said transfer channel region.

50. A method as in claims 25, 26, or 27 which further comprises the step of forming a tunnel oxide on only the edges of said first floating gate and said second floating gate adjacent to said transfer channel region to serve as said tunneling zones, comprising the steps of:

forming a plurality of polycrystalline silicon strips;

forming a second layer of polycrystalline silicon above and insulated from said first layer of polycrystalline silicon;

patterning said second layer of polycrystalline silicon to form said plurality of said first and second control gates;

patterning said first layer of polycrystalline silicon to remove portions of said first layer of polycrystalline silicon between adjacent pairs of said first and second control gates;

forming spacer dielectric on the exposed side walls of said first and second polycrystalline silicon layers;

removing exposed portions of said first polycrystalline silicon layer;

forming tunnel oxide on the exposed side walls of said first polycrystalline silicon layer; and

forming a third layer of polycrystalline silicon.

51. A method as in claim 50 wherein a portion of said first and second channel regions adjacent said source regions and drain regions, respectively, are doped to concentrations greater than that of the remaining portions of said channel regions prior to said step of forming spacer dielectric and said source and drain regions are formed after said step of forming said spacer dielectric.

52. A memory array comprising a plurality of segments, each segment including a subarray comprising:

a plurality of adjacent bit lines running in a first direction to form a corresponding plurality of columns;

a plurality of steering lines running in said first direction;

a plurality of word lines running in a second direction generally perpendicular to said first direction to form a corresponding plurality of rows; and

a plurality of memory cells, each memory cell being associated with the intersection of one of said bit lines and one of said word lines.

53. A structure as in claim 52 wherein said word lines serve as said erase lines.

54. A structure as in claim 53 which includes one or more sectors, each sector containing one or more of said word lines

and their corresponding erase lines, each said sector containing a plurality of memory cells capable of being simultaneously erased.

55. A structure as in claim 53 which includes one or more sectors, each sector containing one or more of said word lines which also serve as erase lines, each said sector containing a plurality of memory cells capable of being simultaneously erased.

56. A method as in claim 52 which further comprises the step of storing one of two or more logical states in said memory cell.

57. A memory array as in claim 52 organized as a virtual ground array.

58. A memory array as in claim 52 which further comprises:

a plurality of diffused lines running in said first direction, serving as said bit lines and forming source and drain regions of said memory cells, each memory cell having a first channel region located adjacent said source region and a second channel region located adjacent said drain region, and a transfer channel region located between its said first and second channel regions;

a plurality of first floating gates, each located above said first channel region of an associated one of said memory cells;

a plurality of second floating gates, each located above said second channel region of an associated one of said memory cells;

a plurality of first control gate lines, running in said first direction, each located above an associated set of said first floating gates and serving as those of said steering lines associated with each said first floating gate;

a plurality of second control gate lines, running in said first direction, each located above an associated set of said

second floating gates and serving as those of said steering lines associated with each said second floating gate; and

a plurality of row lines serving as said word lines, running in said second direction generally perpendicular to said first direction, forming a set of third control gates above said transfer channel regions of each memory cell, overlying at least a portion of associated ones of said first and second control gates and serving as control gates of access transistors of associated memory cells,

wherein each of said memory cells is associated with the intersection of one of said diffused lines and one of said row lines, and

wherein each memory cell includes a first tunnelling zone formed between said first floating gate and said third control gate, and including one or more of edges, side wall, corners of the top edge, portions of the top, and portions of the bottom of said first floating gate, and

wherein each memory cell includes a second tunnelling zone formed between said second floating gate and said third control gate, and including one or more of edges, side wall, corners of the top edge, portions of the top, and portions of the bottom of said second floating gate.

59. A memory array as in claim 58 wherein said one of first or second floating gates in alternate cells in a given row are verified simultaneously.

60. A memory array as in claim 59 wherein an entire row is verified utilizing four verification operations.

61. A memory array as in claim 58 wherein alternate cells in a given row are programmed simultaneously by placing data associated with each memory cell to be programmed on its associated bit line.

62. A memory array as in claim 61 wherein an entire row is programmed utilizing four program operations.

63. A structure as in claims 1, 2, 3, 4, 5, 6, or 52 which further comprises steering bias circuitry capable of providing steering bias voltage levels less than zero.